WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a first dielectric layer over a substrate;

copper (Cu) or a Cu alloy inlaid in the first dielectric layer; and

a composite capping layer on the inlaid Cu or Cu alloy, the composite capping layer comprising:

a layer of beta (β)-tantalum (Ta) on an upper surface of the inlaid Cu or Cu alloy;

a layer of tantalum nitride on the layer of β-Ta; and

a layer of alpha (α)-Ta on the layer of tantalum nitride.

2. The semiconductor device according to claim 1, wherein the composite capping layer is formed in a recess in the inlaid Cu or Cu alloy such that an upper surface of the α-Ta layer is substantially coplanar with an upper surface of the first dielectric layer.

3. The semiconductor device according to claim 2, wherein:

the layer of β-Ta has a thickness of 25Å to 40Å;

the layer of tantalum nitride has a thickness of 20Å to 100Å; and

the layer of α-Ta has a thickness of 200Å to 500Å.

4. The semiconductor device according to claim 1, wherein:

the layer of β-Ta has a thickness of 25Å to 40Å ;

the layer of tantalum nitride has a thickness of 20Å to 100Å; and

the layer of α-Ta has a thickness of 200Å to 500Å.

5. The semiconductor device according to claim 3, further comprising:

a diffusion barrier lining and opening in the first dielectric layer; and

the Cu or Cu alloy on the diffusion barrier filling the opening.

6. The semiconductor device according to claim 3, further comprising:

a second dielectric layer over the first dielectric layer; and

Cu or a Cu alloy inlaid in an opening in the second dielectric layer in electrical contact with the upper surface of the α-Ta layer.

7. The semiconductor device according to claim 6, further comprising an α-Ta diffusion barrier lining the opening in the second dielectric layer.

8. The semiconductor device according to claim 6, wherein the opening in the second dielectric layer, is a dual damascene opening, the method comprising filling the dual

damascene opening with Cu or a Cu alloy to form an interconnect comprising a lower via in contact with an upper line.

9. The method according to claim 8, further comprising a composite capping layer on the Cu or Cu alloy filling the opening in the second dielectric layer, the composite capping layer comprising:

a layer of β-Ta on the Cu or Cu alloy;

a layer of tantalum nitride on the layer of β-Ta; and

a layer of α-Ta on the layer of tantalum nitride.

10. A method of manufacturing a semiconductor device, the method comprising:

forming an opening in a first dielectric layer;

filling the opening with copper (Cu) or a Cu alloy; and

forming a composite capping layer on the Cu or Cu alloy, the composite capping layer comprising:

a layer of beta (β)-tantalum (Ta) on an upper surface of the Cu or Cu alloy;

a layer of tantalum nitride on the layer of β-Ta; and

a layer of alpha (α)-Ta on the layer of tantalum nitride.

11. The method according to claim 10, comprising:

forming a recess in the upper surface of the Cu or Cu alloy before forming the composite capping layer; and

chemical mechanical polishing (CMP) after forming the composite barrier layer such that an upper surface of the α-Ta layer is substantially coplanar with an upper surface of the first dielectric layer.

12. The method according to claim 11, comprising forming a diffusion barrier lining the opening before filling the opening with Cu or a Cu alloy.

13. The method according to claim 11, comprising:

forming the layer of β-Ta at a thickness of 25Å to 40Å;

forming the layer of tantalum nitride at a thickness of 20Å to 100Å; and

forming the layer of α-Ta at a thickness of 200Å to 500Å.

14. The method according to claim 10, comprising:

forming the layer of β-Ta at a thickness of 25Å to 40Å;

forming the layer of tantalum nitride at a thickness of 20Å to 100Å; and

forming the layer of α-Ta at a thickness of 200Å to 500Å.

15. The method according to claim 11, comprising depositing the β-Ta, titanium nitride and α-Ta layers by physical vapor deposition (PVD).

16. The method according to claim 11, further comprising:

forming a second dielectric layer over the first dielectric layer;

forming an opening in the second dielectric layer; and

filling the opening in the second dielectric layer with Cu or Cu alloy in electrical contact with the upper surface of the α-Ta layer of the composite capping layer.

17. The method according to claim 16, comprising lining the opening in the second dielectric layer with an α-Ta diffusion barrier layer before filling the opening with Cu or Cu alloy.

18. The method according to claim 16, wherein the opening is a dual damascene opening, the method comprising filling the dual damascene opening with Cu or Cu alloy to form an interconnect comprising a lower via in contact with an upper line.

19. The method according to claim 18, further comprising forming a composite barrier layer on the Cu or Cu alloy in the opening in the second dielectric layer, the composite barrier layer comprising:

a layer of β-Ta on the Cu or Cu alloy;

a layer of tantalum nitride on the layer of β-Ta; and

a layer of α-Ta on the layer of tantalum nitride.